AMENDMENT

In The Specification:

Please replace the paragraph with the following amended paragraph:

[0023] The frequency selection unit 100 is used to receive an input signal of data or enabling and mode selection signals [[Mod_1]] Mod_2, Mod_3 and export a frequency-selection voltage at a node X, according to the mode selection signals. The frequency selection unit 100 includes, for example, a control circuit 30, and selector switch 32, and a con-stant voltage generator 33. The control circuit 30 receives input signal DATA or ENABLE and mode selection signals [[Mod_1]] Mod_2, Mod_3, and then export a control signal to the selector switch 32. The DATA is either 0 or 1, and the ENABLE signal deter-mines whether or not the modulation signal is transmitted. The selector switch 32 also receives a voltage signal from the constant voltage generator 33. The constant voltage generator 33, for example, can generate five voltage levels in a relation, such as V1 > V2 > V0 > V3 > V4. As described in FIG. 2, the frequency spacing is selected accord-ing to the voltage. For example, (V1 & V2) represent the "0" level, and (V3 & V4) rep-resent the "1" level. V0 is un-modulated voltage before modulation. The desired fre-quency spacing can be obtained by properly adjusting the voltage value. The frequency spacing can be combination of fmi, such as [fm1, fm4], [fm1, fm3], [fm2, fm4] or [fm2, fm3]. The frequency selection unit 100 then exports a signal of frequency-selection voltage at the node X.

[0030] The decoder 46 receives a digital signal with at least one bit. In the example, two bits of Mod_1 and [[Mod_2]] Mod_0 are used for descriptions. The decoder 46 has the output channels b0-b3, which have the number equal to 2n, where n is the input bit number. In the example, n =2. The output channels are respectively coupled to the switching devices 42 and 44 for each diode pairs. The decoder then decodes the quan-tity of the digital signal and applying the enabling signal to the switching devices, ac-cordingly. For example, when the data 00 is received, then the b0 channel is at enable state, and then the switching devices 42, 44 at the first channel are turned on. Then, the capacitance contributed form the diodes is enabled and added to the VCO core 36 (see FIG. 3). Likewise, if the binary digital data 10 is received, then channels b0 and b2 are turned on. The capacitance from the two channels are added together to have another quantity of capacitance.